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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,365	09/25/2003	Gregory Michael Nordstrom	ROC920030212US1	1856

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EXAMINER	
PHAN, RAYMOND NGAN	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,365	NORDSTROM ET AL.	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-31 are pending.

2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2111.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 15 and 30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In this case, program code (claim 15) and program product (claim 30) are directed to non-statutory subject matter..

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 1-31 are rejected under 35 U.S.C. § 102(e) as being anticipated by Pettey et al. (US No. 6,594,712).

In regard to claim 1, Pettey et al. disclose a method of allocating a memory address space to a plurality of Peripheral Component Interconnect (PCI) adapters coupled to a plurality of slots in a PCI bus (see col. 3, lines 52-64), the method comprising: accessing configuration data associated with a slot identifier for each of the plurality of slots to determine a memory range size associated with each slot (see col. 7, lines 52-65); and non-uniformly allocating memory address ranges to the plurality of PCI adapters based upon the memory range sizes associated with each slot (see col. 9, lines 14-34).

In regard to claims 2, 15, 30-31, Pettey et al. disclose a method of allocating memory addresses to a plurality of input/output (IO) resources coupled to a plurality of IO endpoints in a memory mapped IO fabric (see figure 1, col. 6, lines 20-39), the method comprising: determining a location in the memory mapped IO fabric for each IO endpoint among the plurality of endpoints (see col. 9, lines 44-65); and non-uniformly allocating memory address ranges to the plurality of IO endpoints based upon the determined locations of the IO endpoints in the memory mapped IO fabric (see col. 18, line 53 through col. 19, line 23).

In regard to claims 3, 16, Pettey et al. disclose wherein determining the location and non-uniformly allocating memory address ranges are performed during initialization of the memory mapped IO fabric (see col. 7, lines 29-65).

In regard to claims 4, 17, Pettey et al. disclose wherein determining the location and non-uniformly allocating memory address ranges are performed during initialization of a computer to which the memory mapped IO fabric is coupled (see col. 7, lines 29-65).

In regard to claims 5, 18, Pettey et al. disclose wherein the computer comprises a logically-partitioned computer, and wherein determining the location and non-uniformly allocating memory address ranges are performed by a partition manager in the logically-partitioned computer (see col. 7, line 66 through col. 8, line 7).

In regard to claims 6, 19, Pettey et al. disclose wherein allocating memory address ranges to the plurality of IO endpoints includes allocating differently sized memory address ranges to first and second IO endpoints having the same connector type (see col. 7, lines 51-65).

In regard to claims 7, 20, Pettey et al. disclose wherein the first and second IO endpoints each comprise an IO slot, and wherein the connector types of the first and second IO endpoints have the same data bus width (see col. 7, lines 29-44).

In regard to claims 8, 21, Pettey et al. disclose wherein the memory mapped IO fabric comprises a PCI-compatible fabric (see figure 1, col. 6, lines 15-29).

In regard to claims 9, 22, Pettey et al. disclose wherein the memory mapped IO fabric comprises at least one PCI-compatible bus, wherein at least a subset of IO endpoints are IO slots coupled to the PCI-compatible bus, and wherein the

location of each IO slot is defined by a slot identifier for such IO slot on the PCI-compatible bus (see figure 1, col. 6, lines 15-65).

In regard to claims 10, 23, Pettey et al. disclose wherein the memory mapped IO fabric comprises a plurality of PCI-compatible buses, wherein at least a subset of IO endpoints are IO slots coupled to the plurality of PCI-compatible buses, and wherein the location of each IO slot is defined by a bus identifier for the PCI-compatible bus to which such IO slot is coupled, and a slot identifier for such IO slot on the PCI-compatible bus to which such IO slot is coupled (see figure 1, col. 6, lines 15-65).

In regard to claims 11, 24-25, Pettey et al. disclose wherein the memory mapped IO fabric comprises a plurality of IO enclosures, each IO enclosure including at least one PCI-compatible bus among the plurality of PCI-compatible buses, wherein determining the location of an IO endpoint comprises accessing configuration data associated with the IO enclosure within which such IO endpoint is disposed (see figure 1, col. 6, lines 15-55).

In regard to claim 12, 26, Pettey et al. disclose wherein a PCI-compatible bus among the plurality of PCI-compatible buses includes a PCI-compatible host bridge (see figure 1, col. 6, lines 15-55), the method further comprising allocating a memory address range to the PCI-compatible host bridge (see col. 9, liens 44-65), wherein non-uniformly allocating memory address ranges to the plurality of IO endpoints includes allocating memory address ranges to a plurality of IO slots coupled to the PCI-compatible host bridge from the memory address range allocated to the PCI-compatible host bridge (see col. 9, lines 14-65).

In regard to claims 13, 27, Pettey et al. disclose wherein non-uniformly allocating memory address ranges to the plurality of IO slots includes allocating a

remaining memory address range to a last IO slot among the plurality of IO slots, wherein the remaining memory address range comprises that portion of the memory address range allocated to the PCI-compatible host that was not allocated to each other IO slot among the plurality of IO slots (see col. 9, lines 14-65).

In regard to claims 14, 28, Pettey et al. disclose wherein the IO fabric includes at least one IO fabric element allowing connectivity to a subset of the plurality of IO endpoints (see figure 1), and wherein the memory address ranges that would be allocated to IO resources coupled to each IO endpoint in the plurality of IO endpoints are determinable from a publication available prior to installation of IO resources in the subset of IO endpoints (see col. 9, lines 14-65).

In regard to claim 29, Pettey et al. disclose the plurality of IO resources and the memory mapped IO fabric (see figure 1).

Conclusion

8. All claims are rejected.

9. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Biran et al. (US No. 6,658,521) disclose a method and apparatus for address translation on PCI bus over infiniband network.

Horan et al. (US No. 5,999,743) disclose system and method for dynamically allocating accelerated graphics port memory space.

Campbell et al. (US No. 6,526,459) disclose an allocation of input/output bus address space to native input/output devices.

Blackledge et al. (US No. 5,835,738) disclose an address space architecture for multiple bus computer system.

Langendorf et al. (US No. 6,823,418) disclose a virtual PCI device apparatus and method.

Surugucchi et al. (US No. 6,094,699) disclose an apparatus and method for coupling devices to a PCI-to-PCI bridge in an intelligent I/O controller.

Dearth et al. (US No. 6,854,032) disclose a system for accessing a region of memory using remote address translation and using a memory window table and a memory region table.

Berry (US Pub No. 2002/0078271) discloses method and apparatus for multi-level translation and protection table.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (571) 272-3639 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to **[raymond.phan@uspto.gov]**.

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see hop://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

Raymond Phan
Sept 20, 2005

PAUL R. MYERS
PRIMARY EXAMINER